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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,654	12/20/2001	Jeffrey A. Benis	10019880-1	2726

7590 11/30/2005

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EXAMINER	
GEBRESILASSIE, KIBROM K	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,654	BENIS, JEFFREY A.	
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on 20 December 2001

2. Claims 1-27 have been examined and rejected.

Oath/Declaration

3. The Office acknowledges receipt of a properly signed oath/declaration filed on 20 December 2001.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-27 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,826,061 issued to Walp et al.

As per Claim 1:

Walp discloses a method for simulating an array of flip flops including metastable effects, said method comprising: a) receiving a first set of values comprising a bit value for each flip flop in a first rank of flip flops in said array, wherein said first set of values represents input values for said first rank (col. 5 lines 52-56); and b) computing an input value for each flip flop in a second rank of flip flops in said array by selecting between a respective bit value from said first set of values and a respective bit value from a second set of values, wherein said second set of values represents bit values previously held by flip flops in said first rank (col. 8 lines 32-40); wherein said second rank receives a combination of bit values from said first and second sets of values to simulate said metastable effects (col. 1 lines 59-63).

As per Claim 2:

Walp discloses receiving information defining a width and depth of said array, wherein said width defines the number of flip flops in each rank of said array and wherein said depth defines the number of ranks in said array (Fig. 4A and Fig. 4B).

As per Claim 3:

Walp discloses array represents a plurality of chains of flip flops, wherein the number of flip flops in a chain corresponds to said depth and wherein the number of chains corresponds to said width (Fig. 4A elements 86, 88, and 94).

As per Claim 4:

Walp discloses steps a)-b) are performed for each of a plurality of simulated clock pulses (col. 7 lines 7-47; Fig. 3).

As per Claim 5:

Walp discloses steps a)-b) are performed at an edge of a simulated clock pulse (col. 7 lines 12-17).

As per Claim 6:

Walp discloses generating a random number based on a seed number (col. 6 lines 45-51); and selecting between a bit value from said first set of values and a bit value from said second set of values using said random number (col. 6 lines 38-40).

As per Claim 7:

The limitation of claim 7 has already been discussed in the rejection of claim 4 and claim 6. It is therefore rejected under the same rationale.

As per Claim 8:

Walp fails expressly to disclose synthesizing is selectively turned on and off during said simulating. However, this feature is, which is synthesizing is selectively turned on and off during said simulating, deemed to be inherent to the Walp system as col. 6 lines 38-40 show setting

the output to either low voltage/logical zero or high voltage/logical one accurately simulates the behavior of a metastable state machine, which can be interpreted as selectively turned on and off during simulation. Therefore, the Walp system would be inoperative if the flip-flops are not selectively turned on and off during the simulation in order to find out metastable effects.

As per Claim 9:

The limitation of claim 9 has already been discussed in the rejection of claim 8. It is therefore rejected under the same rationale.

As per Claim 10:

Walp discloses a computer system comprising: a memory unit (col. 2 line 54); and a processor, said processor for executing a method for simulating an array of flip flops including metastable effects (col. 3 lines 64-66), said method comprising: a) receiving a first set of values comprising a bit value for each flip flop in a first rank of flip flops in said array, wherein said first set of values represents input values for said first rank (col. 5 lines 52-56); and b) computing an input value for each flip flop in a second rank of flip flops in said array by selecting between a respective bit value from said first set of values and a respective bit value from a second set of values, wherein said second set of values represents bit values previously held by flip flops in said first rank (col. 8 lines 32-40); wherein said second rank receives a combination of bit values from said first and second sets of values to simulate said metastable effects(col. 1 lines 59-63).

Walp fails expressly to disclose a bus. However, this feature is, which is a bus, deemed to be inherent to the Walp system as col. 3 lines 34-36 show receiving data and transmitting data, helps for communicating information within units. Without having a bus in the system of Walp, it could be impossible to communicate between a processor, display units and memory units or vise versa.

As per Claims 11 and 20:

The limitations of claims 11 and 20 have already been discussed in the rejection of claim 2. They are therefore rejected under the same rationale.

As per Claims 12 and 21:

The limitations of claims 11 and 20 have already been discussed in the rejection of claim 3. They are therefore rejected under the same rationale.

As per Claims 13 and 22:

The limitations of claims 11 and 20 have already been discussed in the rejection of claim 4. They are therefore rejected under the same rationale.

As per Claims 14 and 23:

The limitations of claims 11 and 20 have already been discussed in the rejection of claim 5. They are therefore rejected under the same rationale.

As per Claims 15 and 24:

The limitations of claims 15 and 24 have already been discussed in the rejection of claim 6. They are therefore rejected under the same rationale.

As per Claims 16 and 25:

The limitations of claims 16 and 25 have already been discussed in the rejection of claim 7. They are therefore rejected under the same rationale.

As per Claims 17 and 26:

The limitations of claims 17 and 26 have already been discussed in the rejection of claim 8. They are therefore rejected under the same rationale.

As per Claims 18 and 27:

The limitations of claims 18 and 27 have already been discussed in the rejection of claim 9. They are therefore rejected under the same rationale.

As per Claim 19:

The limitation of claim 19 has already been discussed in the rejection of claim 1. It is therefore rejected under the same rationale.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Clifford E. Cummings, "Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs", Sunburst Design, Inc., pp 1-26, March 7, 2001.

Jens U. Horstmann, Hans W. Eichel, and Robert L. Coates, " Metastability Behavior of CMOS ASIC Flip-Flops in Theory and Test", 1989 IEEE, Vol. 24, No. 1, pp. 146-157.

Chris Wellheuser, "Metastability Performance of Clocked FIFOs", SCZA004A, Texas Instrument, pp 1-12, 1996.

Rennie W. Dover, "Metastability and the ECLinPS Family", ECL Application Engineering, Semiconductor Components Industries, LLC, October 2000, pp. 1-7.

Lee-Sup Kim, and Robert W. Dutton, "Metastability of CMOS Latch/Flip-Flop", 1990 IEEE, vol. 25, No. 4, pp. 942-951, August 1990.

U.S. Patent No. 4,982,18 issued to Lloyd et al.

U.S. Patent No. 6,408,265 issued to Schultz et al

2. Any inquiring concerning this communication or earlier communication from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is (571) 272-8571. The examiner can normally be reached on Monday-Friday, 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Kamini shah can be reached at (571) 272-2279. The official fax number is (571) 273-8300. Any inquiring of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is (571) 272-3700.

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